Curriculum Vitae

Minsu Choi, Ph.D.

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WORK EXPERIENCE

Associate Professor, Dept of Electrical & Computer Engineering, Missouri S&T, Sep 2009 - Present

Assistant Professor, Dept of Electrical & Computer Engineering, Missouri S&T, 2003 - 2009

EDUCATION

Ph.D. in Computer Science, Oklahoma State University, Aug 02
Dissertation Title: System-on-Chip Design for Reliability
OSU Research Excellence Award Recipient

M.S. in Computer Science, Oklahoma State University, May 98

B.S. in Computer Science, Oklahoma State University, May 95

RESEARCH INTERESTS

High-Performance Computer Architecture, VLSI, Heterogeneous Computing, Trustworthy computing, Embedded Systems, Fault Tolerance, Reliability Modeling and Analysis, Reconfigurable Computing, Parallel & Distributed Systems, and Dependable Instrumentation & Measurement.

PUBLICATIONS

Papers in Refereed Journals

[1] Jong-Seok Lee, Sriram Venkateswaran and Minsu Choi, **Efficient Post-Configuration Testing of Asynchronous Nanowire Crossbar System for Reliability**, *IET Computers & Digital Techniques*, Vol. 6, No. 4, pp. 214 - 222, 2012.

[2] Jun Wu, Yiyu Shi and Minsu Choi, **Measurement and Evaluation of Power Analysis Attacks on Asynchronous S-Box**, *IEEE Transactions on Instrumentation & Measurement*, Vol. 61, No. 10, pp. 2765-2775, 2012.

[3] W. Hong, R. Modugu and M. Choi, **Efficient On-line Self-Checking Modulo 2^n+1 Multiplier Design**, *IEEE Transactions on Computers*, Vol. 60, No. 9, pp. 1354-1365, Sep. 2011.

[4] W. Jun and M. Choi, **Latency/Area Analysis and Optimization of Asynchronous Nanowire Reconfigurable Crossbar System**, *Nano Communication Networks*, Elsevier, Vol. 1, No. 4, pp. 301-309, Dec. 2010.

[5] J. Lee and M. Choi, **Cost-Driven Optimization of Defect-Avoidant Logic Mapping Strategies for Nanowire Reconfigurable Crossbar Architecture**, *Journal of KIISE (Korean Institute of Information Scientists and Engineers) : Computer Systems and Theory*, Vol. 37, No. 5, pp. 257-271, Oct. 2010.

[6] T. Feng, N.-J. Park, M. Choi and N. Park, **Reliability Modeling and Analysis of Clockless Wave Pipeline Core for Embedded Combinational Logic Design**, *IEEE Transactions on Instrumentation & Measurement*, Vol. 59, No. 7, pp. 1812-1824, July 2010.

[7] H. Jeon, Y. Kim and M. Choi, **Standby Leakage Power Reduction Technique for Nanoscale CMOS VLSI Systems**, *IEEE Transactions on Instrumentation & Measurement*, Vol. 59, No. 5, pp. 1127-1133, May 2010.

[8] Yadunandana Yellambalase and Minsu Choi, **Cost-Driven Repair Optimization of Reconfigurable Nanowire Crossbar Systems with Clustered Defects**, *Journal of Systems Architecture (JSA)*, Vol. 54, No. 8. pp. 729 - 741, Aug 2008.

[9] Myungsu Choi and Minsu Choi, **Scalability of Globally Asynchronous QCA (Quantum-Dot Cellular Automata) Adder Design**, *Journal of Electronic Testing: Theory and Applications (JETTA)*, Vol. 24, No. 1 - 3, pp. 313 - 320, Jun 2008.

[10] Kyung Ki Kim, Yong-Bin Kim, Minsu Choi and Nohpill Park, **Leakage Minimization Technique For Nanoscale CMOS VLSI**, *IEEE Design & Test of Computers - Special Issue on Computer Aided Design for Emerging Technologies*, Vol. 24, No. 4, pp. 322 - 330, July-August 2007.

[11] Myungsu Choi, Zachary D. Patitz, Byoungjae Jin, Feng Tao, Nohpill Park and Minsu Choi, **Designing Layout-Timing Independent Quantum-Dot Cellular Automata (QCA) Circuits by Global Asynchrony**, *Journal of Systems Architecture (JSA)*, Vol. 53, No. 9, pp. 551 - 567, Sep 2007.

[12] Shanrui Zhang, Minsu Choi, Nohpill Park and Fabrizio Lombardi, **Cost-Driven Optimization of Fault Coverage in Combined Built-In Self-Test/Automated Test Equipment Testing**, *IEEE Transactions on Instrumentation and Measurement*, Vol. 56, No. 3, pp. 1094 - 1100, June 2007.

[13] Jongwon Park, Chang-Soo Kim and Minsu Choi, **Oxidase-Coupled Amperometric Glucose and Lactate Sensors with Integrated Electrochemical Actuation System**, *IEEE Transactions on Instrumentation and Measurement*, Vol. 55, No. 4, pp. 1348-1355, Aug 2006.

[14] Choi, M., Park, N., Lombardi, F. and Piuri, V. **Reliability Measurement of Mass Storage System for Onboard Instrumentation**, *IEEE Transactions on Instrumentation and Measurement*, Vol. 54, No. 6, pp. 2297-2304, Dec 2005.

[15] Park, N.-J., George, K.M., Park, N., Choi, M., Kim, Y.B. and Lombardi, F., **Environmental-Based Characterization of SoC for Stratified Testing**, *IEEE Transactions on Instrumentation and Measurement*, Vol. 54, No. 3, pp. 1241-1248, June 2005.

[16] Choi, M., Park, N., Piuri, V., Kim, Y.B and Lombardi, F. **Evaluating the Repair of System-on-Chip (SoC) Instrumentation using Connectivity**, *IEEE Transactions on Instrumentation and Measurement*, Vol. 53, No. 6, pp. 1464-1472, Dec 2004.

[17] Liu, B., Lombardi, F., Park, N. and Choi, M., **Testing Layered Interconnection Networks**, *IEEE Transactions on Computers*, Vol. 53, No. 6, pp. 710-722, June 2004.

[18] Choi, M., Park, N., Piuri, V., Kim, Y.B. and Lombardi, F., **Balanced Dual-Stage Repair for Dependable Embedded Memory Cores**, *Journal of Systems Architecture - Special Issue: Design and Test of System on a Chip*, Vol. 50, No. 5, pp. 281-285, April 2004.

[19] Bandapati, S. K., Smith, S. C. and Choi, M., **Design and Characterization of NULL Convention Self-Timed Multipliers**, *IEEE Design & Test of Computers - Special issue on Clockless Digital Circuits*, Vol. 20, No. 6, pp. 26-36, Nov-Dec 2003.

[20] Choi, M., Park, N. and Lombardi, F. **Modeling and Analysis of Fault Tolerant Multistage Interconnection Networks**, *IEEE Transactions on Instrumentation and Measurement*, Vol. 52, No. 5, pp. 1509-1519, October 2003.

[21] Jin, B.J., Park, N., George, K.M., Choi, M. and Yeary, M, **Modeling and Analysis of Soft-Test/Repair for CCD-based Digital X-Ray Systems**, *IEEE Transactions on Instrumentation and Measurement - Special Issue on Reliable Digital Instrumentation, December 2003*, Vol. 52, No. 6, pp. 1713-1721, December 2003.

[22] Park, N.-J., George, K.M., Choi, M., Park, N. and Lee, R. **Distributed Web-Based Computing (DWBC) Models with Caching Resource Utilization (CRU)**, *International Journal of Computer and Information Science (IJCIS)*, International Association for Computer & Information Science, Vol. 4, No. 1, pp. 60-69, March 2003.

[23] Choi, M. and Park, N. **Dynamic Yield Analysis and Enhancement of FPGA Reconfigurable Memory System**, *IEEE Transactions on Instrumentation and Measurement*, Vol. 51, No. 6, pp. 1300-1311, December 2002.

[24] Choi, M., Park, N., Lombardi, F. and Piuri, V. **Quality Enhancement of Reconfigurable Multichip Module Systems by Redundancy Utilization**, *IEEE Transactions on Instrumentation and Measurement*, Vol. 51, No. 4, pp. 740-749, August 2002.

Other Publication Activity in Referred Journals

[1] Minsu Choi, Fabrizio Lombardi and Nohpill Park, **Introduction to the Special Section on Nanocircuits and Systems**, *IEEE Transactions on VLSI*, Vol. 17, No. 4, pp. 470 - 472, April 2009.

Book Chapters

[1] Jun Wu, Sriram Venkateswaran and Minsu Choi **Advances in Nanowire-Based Computing Architectures**, *Cutting Edge Nanotechnology*, ISBN: 978-953-7619-X-X, IN-TECH publishing, pp. 225-252, 2010.

Papers in Refereed Conference Proceedings

[1] Jun Wu, Hengsi Qin, Yiyu Shi, Kyung Ki Kim, Ho Joon Lee, Yong-Bin Kim and Minsu Choi, **Stochastic Encoding for Enhanced Resistance against Power Analysis Attacks in Crypto-Hardware**, *2014 International Industrial Information Systems Conference*, pp. 7-9, Jan 2014.

[2] Byunghyun Jang, Minsu Choi and Kyung-Ki Kim **Algorithmic GPGPU Memory Optimization**, *IEEE International System-On-Chip Conference (ISOCC) 2013*, pp. 154-157, Nov 2013 - Samsung Best Paper Award Winner.

[3] Ronak Shah, Minsu Choi and Byunghyun Jang, **Workload-Dependent Relative Fault Sensitivity and Error Contribution Factor of GPU Onchip Memory Structures**, *IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XIII) 2013*, pp. 271-278, July 2013.

[4] Hui Geng, Jun Wu, Jianming Liu, Minsu Choi and Yiyu Shi, **Utilizing Random Noise in Cryptography: Where is the Tofu (Invited Paper)**, *IEEE International Conference on Computer-Aided Design (ICCAD) 2012*, pp. 163-167, Nov 2012.

[5] He Qi, Yong-Bin Kim and Minsu Choi, **A High Speed Low Power Modulo $2^n + 1$ Multipler Design using Carbon-nanotube Technology**, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) 2012*, pp. 406-409, Aug 2012.

[6] Siva Kotipalli, Yong-Bin Kim and Minsu Choi, **Design and Evaluation of Side Channel Attack Resistant Asynchronous AES Round Function**, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) 2012*, pp. 410-413, Aug 2012.

[7] Jun Wu, Yong-Bin Kim and Minsu Choi, **Configurable Logic Block (CLB) Design for Asynchronous Nanowire Crossbar System**, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) 2012*, pp. 170-173, Aug 2012.

[8] Jun Wu, Yong-Bin Kim and Minsu Choi, **Post-Configuration Repair Strategy for Asynchronous Nanowire Crossbar System**, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) 2012*, pp. 174-177, Aug 2012.

[9] Chunchun Sui, Jun Wu, Yiyu Shi, Yong-Bin Kim, and Minsu Choi, **Random Dynamic Voltage Scaling Design to Enhance Security of NCL S-Box**, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Wp1G-1(02-1021), Seoul, South Korea, August 2011.

[10] In Seok Jung, Yong-Bin Kim, and Minsu Choi, **The Novel Switched-Capacitor DCDC Converter for Fast Response and Reduced Ripple**, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Wa1I-4(04-1006), Seoul, South Korea, August 2011.

[11] Heung Jun Jun, Yong-Bin Kim, and Minsu Choi, **Offset Voltage Analysis of Dynamic Latched Comparator**, *IEEE International Midwest Symposium on Circuits and Systems(MWSCAS)*, Ta1A01(01-1028), Seoul, South Korea, August 2011.

[12] Veeresh Hongal, Raghavendra Kotikalapudi, Yong-Bin Kim, and Minsu Choi, **A Novel Divide and Conquer Testing Technique for Memristor Based Lookup Table**, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Tp1G-3(05-1013), Seoul, South Korea, August 2011.

[13] Inseok Jung, Elizabeth Kim and Minsu Choi, **Learning Nanotechnology Through Crossbar-Based Architecture and Carbon Nanotube(CNT) FETs**, *IEEE International Conference on Microelectronic Systems Education (MSE)*, pp. 60 - 63, San Diego, CA, June 2011.

[14] Jun Wu, Yiyu Shi and Minsu Choi, **FPGA-based Measurement and Evaluation of Power Analysis Attack Resistant Asynchronous S-Box**, *IEEE I2MTC Conference 2011*, pp. 1109-1114, Hangzhou, China, May 2011.

[15] Hoseung Lee, Jaeik Lee, Seungyup Baek, Jae-Cheon Lee and Minsu Choi, **Driving Pathfinding of Unmanned Autonomous Ground Vehicle Using Measurement Data Diffusion**, *IEEE I2MTC Conference 2011*, pp. 1545-1548, Hangzhou, China, May 2011.

[16] Janardhanan Ajit, Yong-Bin Kim and Minsu Choi, **Performance Assessment of Analog Circuits with Carbon Nanotube FET (CNFET)**, *ACM Great Lakes Symposium on VLSI 2010 (GLSVLSI10)*, pp. 163-166, Providence, USA, 2010.

[17] Jun Wu, Yong-Bin Kim and Minsu Choi, **Low-Power Side-Channel Attack-Resistant Asynchronous S-Box Design for AES Cryptosystems**, *ACM Great Lakes Symposium on VLSI 2010 (GLSVLSI10)*, pp. 459 - 464, Providence, USA, 2010.

[18] Jun Wu and Minsu Choi, **Memristor Lookup Table (MLUT)-Based Asynchronous Nanowire Crossbar Architecture**, *IEEE International Conference on Nanotechnology 2010*, pp. 1100-1103, Seoul, Korea, 2010.

[19] Jun Wu and Minsu Choi, **Latency & Area Measurement and Optimization of Clock-Free Nanowire Reconfigurable Crossbars**, *IEEE International Instrumentation and Measurement Technology Conference 2010*, pp. 1596-1601, Austin, USA.

[20] Rajashekhar Modugu and Minsu Choi, **Design and performance measurement of efficient IDEA (International Data Encryption Algorithm) crypto-hardware using novel modular arithmetic components**, *IEEE International Instrumentation and Measurement Technology Conference 2010*, pp. 1222-1227, Austin, USA.

[21] Eun Ki Kim, Noh-Jin Park, Zachary Patitz, Hanbyeong Cho, Minsu Choi and Nohpill Park, **A management of highway emergency vehicle-to-vehicle communication**, *IEEE International Instrumentation and Measurement Technology Conference 2009*, pp. 323 - 327, Singapore, May 5-7, 2009.

[22] Geunho Cho, Minsu Choi, Fabrizio Lombardi and Yong-Bin Kim, **Performance Evaluation of CNFET-Based Logic Gates**, *IEEE International Instrumentation and Measurement Technology Conference 2009*, pp. 909 - 912, Singapore, May 5-7, 2009.

[23] Rajashekhar Modugu, Nohpill Park and Minsu Choi, **A Fast Low-Power Modulo $2^n + 1$ Multiplier Design**, *IEEE International Instrumentation and Measurement Technology Conference 2009*, pp. 951 - 956, Singapore, May 5-7, 2009.

[24] Heung Jun Jeon, Minsu Choi and Yong-Bin Kim, **A Novel Technique to Minimize Standby Leakage Power in Nanoscale CMOS VLSI**, *IEEE International Instrumentation and Measurement Technology Conference 2009*, pp. 1372 - 1375, Singapore, May 5-7, 2009.

[25] Sriram Venkateswaran, Jong-Seok Lee and Minsu Choi, **Novel Functional Testing Technique for Asynchronous Nanowire Crossbar System**, *IEEE International Instrumentation and Measurement Technology Conference 2009*, pp. 1121 - 1125, Singapore, May 5-7, 2009.

[26] Shikha Chaudhary, Yong-Bin Kim and Minsu Choi, **Probabilistic Analysis of Design Mapping in Asynchronous Nanowire Crossbar Architecture**, *IEEE International Instrumentation and Measurement Technology Conference 2009*, pp. 1116 - 1120, Singapore, May 5-7, 2009.

[27] Ravi Bonam and Minsu Choi, **Evaluating Performance Tradeoff in Defect-Tolerant Gate Programming Techniques for the Clock-Free Nanowire Crossbar Architecture**, *IEEE International Conference on Nanotechnology 2008*, Arlington, TX, 18-21 August 2008 - *Invited Presentation*.

[28] Sriram Venkateswaran and Minsu Choi, **Post-Configuration Testing of Asynchronous Nanowire Crossbar Architecture**, *IEEE International Conference on Nanotechnology 2008*, Arlington, TX, 18-21 August 2008.

[29] Ravi Bonam, Yong-Bin Kim and Minsu Choi, **Defect-Tolerant Gate Macro Mapping & Placement in Clock-Free Nanowire Crossbar Architecture**, *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems 2007*, pp. 161-169, Rome, Italy, 26-28 September 2007.

[30] Yadunandana Yellambalase, Ravi Bonam and Minsu Choi, **Redundancy Optimization for Clock-Free Nanowire Crossbar Architecture**, *2007 IEEE Conference on Nanotechnology*, pp. 621-623, Hong Kong, Aug 2-5, 2007.

[31] Ravi Bonam, Shikha Chaudhary, Yadunandana Yellambalase and Minsu Choi, **Clock-Free Nanowire Crossbar Architecture based on Null Convention Logic (NCL)**, *2007 IEEE Conference on Nanotechnology*, pp. 85-89 Hong Kong, Aug 2-5, 2007.

[32] Kyung-Ki Kim, Yong-Bin Kim, Minsu Choi, Nohpill Park and Fabrizio Lombaridi, **Accurate Macro-modeling for Leakage Current for IDDQ Test**, *2007 IEEE Instrumentation and Measurement Technology Conference*, pp. 1-4, Warsaw, Poland, May 1-3, 2007.

[33] B. Jin and N. Park, M. Choi and F. Lombardi, **BIST Design for CCD based Digital Imaging System**, *2007 IEEE Instrumentation and Measurement Technology Conference*, pp. 1-6, Warsaw, Poland, May 1-3, 2007.

[34] Yadunandana Yellambalase and Minsu Choi, **Automatic Node Discovery in CAN (Controller Area Network) Controllers using Reserved Identifier Bits**, *2007 IEEE Instrumentation and Measurement Technology Conference*, pp. 1-3, Warsaw, Poland, May 1-3, 2007.

[35] Kyung-Ki Kim, Jing Huang, Yong-Bin Kim, Fabrizio Lombardi and Minsu Choi, **Analysis and Simulation of Jitter for High Speed Channels in VLSI Systems**, *2007 IEEE Instrumentation and Measurement Technology Conference*, pp. 1-4, Warsaw, Poland, May 1-3, 2007.

[36] Yadunandana Yellambalase, Minsu Choi and Yong-Bin Kim, **Inherited Redundancy and Configurability Utilization for Repairing Nanowire Crossbars with Clustered Defects**, *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems 2006*, pp. 98-106, Arlington/Washington DC, USA, October 4-6, 2006.

[37] Minsu Choi, Myungsu Choi, Zachary Patitz and Nohpill Park, **Efficient and Robust Delay-Insensitive QCA (Quantum-Dot Cellular Automata) Design**, *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems 2006*, pp. 80-88, Arlington/Washington DC, USA, October 4-6, 2006.

[38] Yadunandana Yellambalase, Shanrui Zhang, Nohpill Park and Minsu Choi, **Cost-Driven Repairability Optimization for Nanowire Crossbar Architecture**, *2006 IEEE Conference on Nanotechnology*, Vol. 1, pp. 347-350, Cincinnati, OH, USA, 17-20 June 2006.

[39] Rui Tang, Yong-Bin Kim, Minsu Choi and Fabrizio Lombardi, **Jitter Analysis in High Speed Serial Link Using a PWM Scheme**, *Instrumentation and Measurement Technology Conference (IMTC), 2006.*, pp. 494-497, Sorrento, Italy, 24-27 April 2006.

[40] Yadunandana Yellambalase, Jongwon Park, Chang-Soo Kim, Minsu Choi, Nohpill Park and Fabrizio Lombardi, **Automated Oxidase-Coupled Amperometric Microsensor with Integrated Electrochemical Actuation System for Continuous Sensing of Saccharoids**, *Instrumentation and Measurement Technology Conference (IMTC), 2006.*, pp. 1795-1800, Sorrento, Italy, 24-27 April 2006.

[41] Zachary D. Patitz, Nohpill Park, Minsu Choi and Fred J. Meyer, **QCA-Based Majority Gate Design under Radius of Effect-Induced Faults**, *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems 2005*, pp. 217-228, Monterey, CA, USA, 03-05 Oct 2005.

[42] Minsu Choi and Nohpill Park, **Locally Synchronous, Globally Asynchronous Design for Quantum-Dot Cellular Automata (LSGA QCA)**, *IEEE International Conference on Nanotechnology*, pp. 121-124, Nagoya, Japan, 11-15 July 2005.

[43] B. Jang, M. Choi, N. Park, Y.B. Kim, V. Piuri, and F. Lombardi, **Spare Line Borrowing Technique for Distributed Memory Cores in SoC**, *Instrumentation and Measurement Technology Conference (IMTC), 2005.*, IEEE Instrumentation and Measurement Society, Vol. 1, pp. 43-48, Ottawa, Canada, 17-19 May 2005.

[44] Jongwon Park, Chang-Soo Kim, Shanrui Zhang and Minsu Choi, **Glucose Oxidase (GOD)-Coupled Amperometric Microsensor with Integrated Electrochemical Actuation System**, *Instrumentation and Measurement Technology Conference (IMTC), 2005.*, IEEE Instrumentation and Measurement Society, Vol. 1, pp. 134-138, Ottawa, Canada, 17-19 May 2005.

[45] Minsu Choi and Nohpill Park, **Teaching Nanotechnology by Introducing Crossbar-based Architecture and Quantum-Dot Cellular Automata**, *2005 IEEE International Conference on Microelectronic Systems Education (MSE05)*, IEEE Computer Society, pp. 29-30, Anaheim, CA, 3-4 June 2005.

[46] Minsu Choi, Shanrui Zhang and Nohpill Park, **Modeling Yield of Carbon-Nanotube/Silicon-Nanowire FET-Based Nanoarray Architecture with H-Hot Addressing Scheme**, *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, IEEE Computer Society, pp. 356-364, Cannes, France, 10-13 Oct 2004.

[47] Shanrui Zhang, Minsu Choi, Nohpill Park and Fabrizio Lombardi, **Probabilistic Balancing of Fault Coverage and Test Cost in Combined Built-in Self-Test/Automated Test Equipment Testing Environment**, *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, IEEE Computer Society, pp. 48-56, Cannes, France, 10-13 Oct 2004.

[48] Shanrui Zhang, Minsu Choi and Nohpill Park, **Defect Characterization and Yield Analysis of Array-Based Nanoarchitecture**, *IEEE International Conference on Nanotechnology*, IEEE Nanotechnology Council, pp. 50-52, Munich, Germany, 16-19 Aug 2004.

[49] N.-J. Park, B. Jin, K.M. George, N. Park and M. Choi, **High Confidence Testing For Instrumentation System-on-Chip with Unknown-Good-Yield**, *Instrumentation and Measurement Technology Conference (IMTC), 2004.*, IEEE Instrumentation and Measurement Society, Vol. 2, pp. 1478-1483, Como, Italy, 18-20 May 2004.

[50] Shanrui Zhang, Minsu Choi, Nohpill Park and Fabrizio Lombardi, **Cost-Driven Optimization of Fault Coverage in Combined Built-In Self-Test/Automated Test Equipment Testing**, *Instrumentation and Measurement Technology Conference (IMTC), 2004.*, IEEE Instrumentation and Measurement Society, Vol. 3, pp. 2021-2026, Como, Italy, 18-20 May 2004.

[51] Park, N.-J., George, K.M., Park, N., Choi, M., **Regressive Testing for System-on-Chip with Unknown-Good-Yield**, *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, IEEE Computer Society, pp. 393-400, Boston, MA, 3-5 Nov. 2003.

[52] Choi, M., Park, N., Lombardi, F., Kim, Y.B. and Piuri, V., **Optimal Spare Utilization in Repairable and Reliable Memory Cores**, *IEEE International Workshop on Memory Technology, Design and Testing, 2003 (MTDT 03)*, IEEE Computer Society, pp. 64-71, San Jose, CA, 28-29 July 2003.

[53] Choi, M., Pottinger, H.J., Park, N. and Kim, Y.B., **Need for Undergraduate and Graduate-Level Education in Testing of Microelectronic Circuits and Systems**, *2003 IEEE International Conference on Microelectronic Systems Education (MSE03)*, IEEE Computer Society, pp. 121 -122, Anaheim, CA, 1-2 June 2003.

[54] Park, N.-J., George, K.M., Park, N., Choi, M., Kim, Y.B. and Lombardi, F., **Environmental-Based Characterization of SoC for Stratified Testing**, *Instrumentation and Measurement Technology Conference (IMTC), 2003.*, IEEE Instrumentation and Measurement Society, pp. 327 -332, vol. 1, Vail, CO, 20-22 May 2003.

[55] Jin, B.J., Park, N., George, K.M., Choi, M., Yeary, M., Kim, Y.B. and Lombardi, F., **Soft-Test/Repair of CCD-based Digital X-Ray Instrumentation**, *Instrumentation and Measurement Technology Conference (IMTC), 2003.*, IEEE Instrumentation and Measurement Society, pp. 315 -320, vol. 1, Vail, CO, 20-22 May 2003.

[56] Choi, M., Park, N., Piuri, V., Kim, Y.B and Lombardi, F. **Evaluating the Repair of System-on-Chip (SoC) Instrumentation using Connectivity**, *Instrumentation and Measurement Technology Conference (IMTC), 2003.*, IEEE Instrumentation and Measurement Society, pp. 309 -314, vol. 1, Vail, CO, 20-22 May 2003.

[57] Choi, M., Park, N.-J., George, K.M., Jin, B., Park, N. and Kim, Y.B., **Fault-Tolerant Memory Design for HW/SW Co-Reliability in Massively Parallel Computing Systems**, *IEEE International Symposium on Network Computing and Applications 03' (NCA-03)*, pp 341 - 348, Boston, MA, Apr 16-18, 2003.

[58] Park, N.-J., George, K.M., Choi, M., Park, N. and Lee, R., **WWW-based Distributed Computing Models for Microsoft .NET Framework**, *2nd Annual International Conference on Computer and Information Science (ICIS '02)*, ACIS , 8-9 August, 2002.

[59] Choi, M., Park, N., Kim, Y., and Lombardi, F. **Hardware/Software Co-Reliability of Configurable Digital Systems**. *PRDC 2002, Pacific Rim International Symposium on Dependable Computing*, IEEE Computer Society, pp. 67-74, Tsukuba, Japan, 16-18 Dec. 2002.

[60] Choi, M., Park, N., Lombardi, F., Kim, Y.B. and Piuri, V. **Balanced Redundancy Utilization in Embedded Memory Cores for Dependable Systems**, *17th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, IEEE Computer Society, pp. 419-427, Vancouver, Canada, 6-8 Nov. 2002.

[61] Chang, Y., Choi, M., Park, N., and Lombardi, F. **Repairability Evaluation of Embedded DRAMs with Multiple Regions**, *17th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, IEEE Computer Society, pp. 428-436, Vancouver, Canada, 6-8 Nov. 2002.

[62] Choi, M., Park, N. and Lombardi, F. **Hardware-Software Co-Reliability in Field Reconfigurable Multi-Processor-Memory Systems**, *Proceedings of International Parallel and Distributed Processing Symposium (IPDPS 2002)*, IEEE Computer Society, pp. 138-151, Fort Lauderdale, Florida, 15-19 April, 2002.

[63] Choi, M., Park, N., George, K.M. and Piuri, V. **Redundancy Optimization of Fault Tolerant Mass Storage Memory for Massively Parallel Computing Systems**, *The 4th International Conference on Massively Parallel Computing Systems*, Euromicro, Ischia, pp. 51-59, Italy, 10-12 April, 2002.

[64] Kim, E.K., Park, N., Choi, M. and Tamura, S. **Cancellation of MRI Motion Artifact in Image Plane**, *Instrumentation and Measurement Technology Conference (IMTC), 2002. Proceedings of the 19th IEEE*, IEEE Instrumentation and Measurement Society, pp. 329 -334, Anchorage, Alaska, 21-23 May 2002.

[65] Choi, M., Park, N., Meyer, F. and Lombardi, F. **Performance Analysis of Fault-Tolerant Multistage Interconnection Networked Parallel Instrumentation with Concurrent Testing and Diagnosis**, *Instrumentation and Measurement Technology Conference (IMTC), 2002. Proceedings of the 19th IEEE*, IEEE Instrumentation and Measurement Society, pp. 1481 -1486, Anchorage, Alaska, 21-23 May 2002.

[66] Choi, M., Park, N., Meyer, F., Lombardi, F. and Piuri, V. **Reliability Measurement of Fault-Tolerant Onboard Memory Systems under Fault Clustering**, *Instrumentation and Measurement Technology Conference (IMTC), 2002. Proceedings of the 19th IEEE*, IEEE Instrumentation and Measurement Society, pp. 1161 -1166, Anchorage, Alaska, 21-23 May 2002.

[67] Choi, M., Park, N., Meyer, F. and Lombardi, F. **Connectivity-Based Multichip Module Repair**, *Proceedings of the 2001 Pacific Rim International Symposium on Dependable Computing*, 2001. IEEE Computer Society, pp. 19-26, Seoul, Korea, 17-19 Dec. 2001.

[68] Choi, M., Park, N., Lombardi, F. and Piuri, V. **Quality Enhancement of Reconfigurable Multichip Module Systems by Redundancy Utilization**, *Instrumentation and Measurement Technology Conference (IMTC), 2001. Proceedings of the 18th IEEE*, IEEE Instrumentation and Measurement Society, pp. 204 -209, vol. 1, Budapest, Hungary, 21-23 May 2001.

[69] Choi, M. and Park, N. **Dynamic Yield Analysis and Enhancement of FPGA Reconfigurable Memory System**, *Instrumentation and Measurement Technology Conference (IMTC), 2001. Proceedings of the 18th IEEE*, IEEE Instrumentation and Measurement Society, pp. 386 -391, vol. 1, Budapest, Hungary, 21-23 May 2001.

PROFESSIONAL ACTIVITIES

Journal Editorship

IEEE Transactions on VLSI - Special Issue on Design of Nano Circuits and Systems, Guest editor (with N. Park at Oklahoma State University and F. Lombardi at Northeastern University), Vol. 17, No. 4, Apr 2009.

Journal of Electronic Testing: Theory and Applications (JETTA) - Special Double Issue on Defect and Fault Tolerance, Guest editor (with N.A. Touba at U of Texas - Austin and A. Salsano at U of Rome, Italy), Vol.25, No. 1-3, Jun 2007.

International Conference Organizer

Program Committee Member, *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, 2004 - Present

Program Committee Member, *IEEE International Conference on Microelectronic Systems Education*, 2005 - Present

Program Committee Member, *ACM-IEEE Great Lakes Symposium on VLSI*, 2011 - Present

Program Committee Member, *IT (Information Technology) Symposium of UKC (US-Korea Conference)*, 2007 - Present

Session Chair, Circuits and Architectures II, *IEEE Conference on Nanotechnology*, 2005

Session Chair, Imaging System and Image Reconstruction I and II, *IEEE Instrumentation and Measurement Technology Conference*, 2003

Technical Reviewer

Paper Reviewer, *IEEE Transactions on Computers*.

Paper Reviewer, *IEEE Transactions on Instrumentation and Measurement*.

Paper Reviewer, *IEEE Transactions on Very Large Scale Integration (VLSI)*.

Paper Reviewer, *IEEE Transactions on Reliability*.

Paper Reviewer, *IEEE Transactions on Education*.

Paper Reviewer, *IEEE Sensors Journal*.

Paper Reviewer, *IEEE Design & Test of Computers*.

Paper Reviewer, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*.

Paper Reviewer, *ACM Journal of Emerging Technologies in Computing (JETC)*.

Paper Reviewer, *IET Circuits, Devices & Systems*.

Paper Reviewer, *Journal of Electronic Testing: Theory and Applications (JETTA)*.

Paper Reviewer, *Journal of Systems Architecture (JSA)*.

Paper Reviewer, *Integration: The VLSI Journal*.

Paper Reviewer, *International Journal of Parallel and Distributed Systems and Networks*.

Paper Reviewer, *Journal of Computer Science and Technology*

Paper Reviewer, *International Journal of Computers and Their Applications*

Paper Reviewer, *International Journal of General Systems*

Paper Reviewer, *Measurement Science & Technology - An Institute of Physics Journal*

Paper Reviewer, *IEEE International Conference on Circuits and Systems (ISCAS)*, 2012 - Present

Paper Reviewer, *ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, 2011 - Present

Paper Reviewer, *IEEE International Conference on Microelectronic Systems Education*, 2005 - Present

Paper Reviewer, *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, 2003 - Present

Paper Reviewer, *IEEE Workshop on High Performance Switching*, 2005

Paper Reviewer, *IEEE Pacific Rim International Symposium on Dependable Computing*, 2001

Book Reviewer

Embedded System Design with C805 - 1st Edution, ISBN: 0495471747, Han-Way Huang, Cengage Learning, Jan 2008 - scheduled to be available in Dec 2008.

Panel Reviewer

Proposal review panelist - NSF, ECCS, Director: Dr. George Haddad Jan, 2014.

Proposal reviewer - Israel Science Foundation (ISF), Feb, 2012.

Proposal review panelist - NSF, ECCS, Feb, 2011.

Proposal review panelist - NSF, ECCS-IHCS-Cyber Systems Panel, Director: Dr. Scott Midkiff, Jan 26-27, 2009.

Proposal review panelist - NSF, NER (Nanoscale Exploratory Reserach) Panel, Director: Dr. Sankar Basu, March 10-11, 2005.

Proposal review panelist - UM Research Board, 2005, 2006, 2007 and 2008.

Proposal review panelist - NSF, ECS (Electrical & Communications Systems) Unsolicited Proposals Panel, Director: Dr. Vittal Rao, December 9-10, 2004.

Proposal review panelist - Korea Research Foundation (Hakjin), 2004.

Media Coverage

Research Highlight: Clock-Free Nanocomputing Architecture - Missouri S&T Researchers Investigate Innovative Clock-Free Nanocomputing Architecture, GradVision published by Council of Graduate Students, Vol. 1, No. 1, MST, Feb 2009.

Officer in Professional Organizations

President, KSEA (Korean-American Scientists and Engineers Association) Rolla Chapter, Jan 2007 - 2010.

Communications Chair, KOCSEA (Korean Computer Scientists and Engineers Association in America), Aug 2006 - July 2007.

President, IEEE Rolla Subsection of St. Louis Section, Jan 2005 - Dec 2005.

Vice President, IEEE Rolla Subsection of St. Louis Section, Jan 2004 - Dec 2004.

Treasurer/Secretary, IEEE Rolla Subsection of St. Louis Section, Jan 2003 - Dec 2003.

STUDENTS SUPERVISED

Advisor, Harshal Govind, MS, in progress.

Advisor, Naveen Kurapati, MS, in progress.

Advisor, Manoj Vishwanathan, MS, in progress.

Advisor, Ronak Shah, MS, in progress.

Advisor, Jun Wu, Ph.D., SU2012, Algotochip.

Advisor, Siva Pavan Kotipalli, MS, SP2012, Samsung Electronics, Austin, TX.

Advisor, Veeresh Hongal, MS, SU2011, Intel.

Advisor, Rajashekar Modugu, MS, FS2010. The 1st Prize Winner of 2009 Missouri S&T Graduate Council Research Showcase (Presentation Title : A Fast Low-Power Modulo $2^n + 1$ Multipler), AMD.

Advisor, Jeffery Ahrendts, Minority undergrad research assistant, The 3rd place winner (w/ $250 cash prize and award certificate) of 2010 Missouri S&T Undergraduate Research Conference - Engineering Area Oral Presentation Competition (Presentation Title: Latency & Area Measurement and Optimization of Asynchronous Nanowire Crossbar Systems).

Advisor, Sriram Venkateswaran, MS, FS2008.

Advisor, Shikha Chaudhary, Probabilistic Analysis of Defect Tolerance in Asynchronous Nano Crossbar Architecture, MS, FS2008, Intel.

Advisor, Vamshi Kadiyala, Non-thesis option, MS, SS2008.

Advisor, Gi-Young Kim, Non-thesis option, MS, SP2008, Korean Army officer.

Advisor, Ravi Bonam, Asynchronous Nanowire Crossbar Architecture for Manufacturability, Modularity and Robustness, MS, SP2008, SUNY-Albany PhD.

Advisor, Yadunandana Yellambalase, Defect Avoidance in Nano Crossbar Architecture, MS, SP2007, Garmin.

Advisor, Shanrui Zhang, Cost-Driven Optimization of Repair Strategies for Tolerating Defective Crosspoints in NanoFabric, MS, SP2005, Intel.

Committee member, Antonio Sabatini, MS Advisor: Dr. Sahra Sedigh, Spring 2014.

Committee member, Tameem Ahmed Khan, MS Advisor: Dr. Hai Xiao, Summer 2013.

Committee member, Rongbo Yang, MS Advisor: Dr. Yiyu Shi, Summer 2013.

Committee member, Arun Gunasekaran, MS Advisor: Dr. Sahra Sedigh, Fall 2012.

Committee member, He Qi, MS Advisor: Dr. Yong-Bin Kim at Northeastern University, Spring 2012.

Committee member, Chi-Cheng Niu, MS Advisor: Dr. Yiui Shi, Fall 2011.

Committee member, Lin Jing, Ph.D, Advisor: Dr. Sahra Sedigh, Fall 2011.

Committee member, Jongwon Park, Ph.D, Advisor: Dr. Chang-Soo Kim, Sep 2009 .

Committee member, Vikram Reddy Surendra, MS, in progress.

Committee member, Srikanth Beerla, MS, in progress.

Committee member, Mendar Joshi, MS, 2008.

Committee member, Nitin Radhakrishnan, MS, 2007.

Committee member, Bonita Bhaskaran, Ph.D., 2007.

Committee member, Venkat Satagopan, Ph.D., 2007.

Committee member, Vipin Sharma, MS, 2007.

Committee member, Valerio Plassi, MS, 2006.

Committee member, Pavankumar Changrasekhar, MS, 2006.

Committee member, Arun Balasubramanian, MS, 2005.

Committee member, Sareen Davireddy, MS, 2003.

VISITING SCHOLARS SPONSORED

Dr. Geon-Woong Kim, Professor, Electrical & Computer Engineering Department, Mokpo Maritime University, Korea, Feb 2009 - Jan 2010.

Dr. Jong-Seok Lee, Professor, Computer Engineering & Education Department, Woosuk University, Korea, Aug 2007 - Feb 2009.

TEACHING AND ADVISING IMPROVEMENT

Attended and presented at 2005 IEEE International Conference on Microelectronic Systems Education (MSE05), Anaheim, CA, 3-4 June 2005.

Participant, UM New Faculty Teaching Scholars Program (NFTS), Aug 2003 - May 2004.

Participant, UMR Freshman Faculty Forum (FFF), Aug 2002 - May 2003.

Attended ASME/AiChE/IEEE Essential Teaching Seminars for Engineering Faculty, Cal Poly, Pomona, CA, 3/27/03 - 3/29/03.

Blackboard course development workshop, 2002.

Grants.gov proposal submission training, March 16 2006.

UNIVERSITY SERVICE

Tang endowed professorship search committee member, 2012 - on-going search.

CpE assistant professorship search committee member, 2010 - Dr. Yiyu Shi hired.

CpE PhD qualifying exam coordinator, 2007 - Present.

Co-Faculty Advisor (with Dr. Maciej Zawdoniak), IEEE Student Branch at Missouri S&T, 2010 - Present.

Co-Faculty Advisor (with Dr. Dan Lin of CS Dept), IEEE Computer Society Student Branch at Missouri S&T, 2009 - 2010.

Faculty Advisor, Korean Student Association, Missouri S&T, 2005 - 2009.

Phonathon faculty volunteer of Electrical & Computer Engineering, 2004 - 2008.

GTA workshop faculty evaluator, Jan 2003.

FE (Fundamentals Engineering) exam faculty proctor, Oct 26th 2003.

HONORS

Samsung Best Paper Award, ISOCC, 2013.

Outstanding Teaching Award, MST, 2007-08.

Outstanding Teaching Award, UMR, 2006-07.

Outstanding Advisor Award, Nominee, UMR, 2007.

Research Excellence Award, Oklahoma State University, August 2002.

Korean Consulate Honor Scholarship, 2001.

Don and Sheley Fisher Scholarship, 2000.

MEMBERSHIPS

Senior Member (since 2008 - Member since 2002), IEEE.

Member, Sigma Xi.

Member, Golden Key International Honor Society.

Member, KSEA (Korean-American Scientists and Engineers Association).

Member, KOCSEA (Korean Computer Scientists and Engineers Association in America).

Member, KAUPA (Korean-American University Professors Association).